REMARKS

This application has been carefully reviewed in light of the Office Action dated June 7, 2004. Claims 1-3 and 6-7 remain in this application. Claims 1 and 2 are the independent claims. Claim 1 has been amended. Claims 4-5 have been cancelled without prejudice. It is believed that no new matter is involved in the amendments or arguments presented herein. Reconsideration and entrance of the amendment in the application are respectfully requested.

Art-Based Rejections

Claims 1-3 and 6-7 were rejected under 35 U.S.C. §103(a) over Yazawa (JP404339500A) in view of Rao (USPN 6,665,409 B1). Claim 3 was rejected under 35 U.S.C. §103(a) over Yazawa (JP404339500A) in view of Rao (USPN 6,665,409 B1) and further in view of Takegahara et al. (USPN 5,228,059). Applicant respectfully traverses the rejections and submits that the claims herein are patentable in light of the clarifying amendments above and the arguments below.

The Yazawa Reference

Yazawa is directed to down-sampling an audio input signal for writing to a delay RAM so that the written data quantity is reduced. According to Yazawa, the data is read out of the delay RAM and subjected to over-sampling for output as an audio output signal. *(See Yazawa, Abstract).*

The Rao Reference

Rao is directed to a method of producing reverberation effects. A filter models early acoustic reflections in response to an input signal. The filter includes a delay buffer of a selected length, a selected number of taps for tapping samples of corresponding amounts of delay, and a summer for summing the tapped samples to

generate a filter output signal. A reverberator models late acoustic reflections and receives the filter output for generating a plurality of output signals. *(See Rao, Col. 1, line 64 to Col. 2, line 7).*

The Takegahara Reference

Takegahara is directed to a code transmission system that converts successive three bits of a binary code into two symbols of a tertiary code. On a sending side, successive three bits of the binary code are arranged in a matrix of three rows and three columns, wherein a row consists of a first symbol of two symbols of the tertiary code, and a column consists of a second symbol of the two symbols of the tertiary code in accordance with a Gray code. On a receiving side, three steps of threshold level are provided for decoding the tertiary code. *(See* Takegahara, *Col. 4, lines 34-46).*

The Claims are Patentable Over the Cited References

The present application is generally directed to a method of processing digital surround-sound data.

As defined by independent Claim 1, a method of generating surround-sound data includes providing a memory which has a sufficient storage capacity for storing a number of bits of data required to maintain a surround-sound for a maximum anticipated delay time. The method includes supplying an instruction delay time voluntarily adjustable within a range of anticipated delay time. The method includes determining the number of compression bits based on the instruction delay time and the storage capacity. The method includes compressing digital input/output signal to a compressed digital signal with the determined number of compression bits to thereby supply the compressed digital signal to the memory. The method includes outputting the compressed digital signal retrieval from the

memory the instruction delay time later as expanded digital signal after expanding. The method includes adding the digital input signal and the expanded digital signal to output as the digital output signal.

The applied references do not disclose or suggest the above features of the present invention as defined by amended independent Claim 1. In particular, the applied references do not disclose or suggest, "determining the number of compression bits based on said instruction delay time and said storage capacity," as required by amended independent Claim 1. In addition, the applied references do not disclose or suggest, "compressing digital input/output signal to a compressed digital signal with the determined number of compression bits, thereby supplying the compressed digital signal to said memory," as further required by amended independent Claim 1. Moreover, the applied references do not disclose or suggest, "outputting said compressed digital signal retrieved from said memory said instruction delay time later as expanded digital signal after expanding," as further required by amended independent Claim 1.

The Yazawa reference is directed to down-sampling an audio input signal for writing to a delay RAM so that the written data quantity is reduced. *(See Yazawa, Abstract).* In general, down-sampling reduces the data size by eliminating (lopping off) a portion of the original data and decreases the resolution of the audio input signal, which reduces the quality of the audio input signal. In addition, Yazawa is further directed to over-sampling the written data from the delay RAM for output as an audio output signal. *(See Yazawa, Abstract).* In general, over-sampling involves interpolation of data for the eliminated (lopped-off) portion of the original signal such that an estimated value between known values is calculated, which often introduces error in the form of distortion for audio signals.

On page 3, the Final Office Action purports that Rao discloses that the compression is determined based on the delay time and storage capacity, wherein a different delay time (i.e. storage capacity) is in relation to the sampling frequency (i.e. bits) of the device. However, this "sampling frequency of the device" is equivalent to "lopping-off by a down-sampling converter" and "interpolating by an over-sampling converter" as described above with reference to Yazawa. In general, "the sampling frequency" and "bits" are substantially different from each other with respect to methods of compressing and expanding data.

In contrast to Yazawa and Rao, the present invention requires compressing a digital input/output signal to a compressed digital signal with the determined number of compression bits, wherein the number of compression bits is based on the instruction delay time and the storage capacity, as recited in independent Claim 1 and supported throughout the specification. The amount of data is reduced by determining the number of compression bits based on the instruction delay time and the storage capacity, as further required by independent Claim 1. The number of compression bits is set such that a larger number of compression bits is set step-wise (e.g. 4 bits, 6 bits, 8 bits, etc.) for a shorter instruction delay time based on the number of compression bits when said instruction delay time is a maximum delay time. The memory can be effectively utilized within a given capacity in storing larger bits of data through adjustment of the data bits of the output of the compression means based on the delay time. Allowing larger data bits can reduce the degradation of the surround-sound signal. *(See Specification; Figure 7; Page 7, line 27 to Page 8, line 3; Page 11, line 11 to Page 12, line 22).*

The ancillary Rao and Takegahara references do not remedy the deficiencies of the primary Yazawa reference. In fact, the applied references, alone or in any combination, do not disclose or suggest the above features as required by amended

independent Claim 1. As an initial matter, Takegahara is specifically directed to a transmission system that converts three successive bits of a binary code into two symbols of a tertiary code.

The Office Action purports that the applied references teach the above combination of features of the present invention by merely stating that the above combination "would have been obvious" to one of ordinary skill in the art.

However, as MPEP §2143.01 makes clear, "the mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination." Id. (*citing In re Mills, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990)*). It is respectfully submitted that the applied references do not teach or suggest the combination of the above references. Moreover, the applied references do not teach or suggest any reasonable expectation of success of such a combination.

Therefore, since the applied references fail to disclose, teach, or suggest the above features as required by independent Claim 1, those references cannot be said to anticipate nor render obvious the invention which is the subject matter of independent Claim 1.

Accordingly, independent Claim 1 is believed to be in condition for allowance and such allowance is respectfully requested.

The Applicant respectfully submits that independent Claim 2 is patentable over the applied references for at least the same reasons as those discussed above with reference to independent Claim 1.

The remaining Claims 3 and 6-7 depend either directly or indirectly from independent Claims 1 and 2 and recite additional features of the invention which are neither disclosed nor fairly suggested by the applied references. Thus, the

remaining Claims 3 and 6-7 are also believed to be in condition for allowance and such allowance is respectfully requested.

Conclusion

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6809 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

Date: August 17, 2004

By: _____
Troy M. Schmelzer
Registration No. 36,667
Attorney for Applicant(s)

500 South Grand Avenue, Suite 1900
Los Angeles, California 90071
Phone: 213-337-6700
Fax: 213-337-6701